Patent claims

1. An interference suppression device for an electronic appliance having a plug device, which has at least one plug element and is arranged on an electrically conductive housing of the electronic appliance, having a printed circuit board, which is arranged in the housing and bears an electrical and/or electronic circuit to which the plug element is connected, and having a capacitor which is connected on the one hand to the plug element and on the other hand to the potential of the housing, characterized in that the capacitor (19, 22) is arranged on the printed circuit board (5), one part (9) of which protrudes out of the housing interior (4) through an opening (3), and likewise extends from the housing interior (4) to the housing exterior (10), and in that the plug element (8) on that part (9) of the printed circuit board (5) which is located in the housing exterior (10) is conductively connected to the capacitor (19, 22) and the circuit.

2. The interference suppression device as claimed in claim 1, characterized in that the capacitor (19) comprises a first and a second capacitor face (18, 12) which are arranged opposite one another such that they are separated by an insulating layer (17), the first capacitor face (18) being electrically conductively connected to the potential of the housing (1), and the second capacitor face (12) being electrically conductively connected to the circuit.

3. The interference suppression device as claimed in claim 2, characterized in that the insulating layer (17) is formed by the printed circuit board (5).

4. The interference suppression device as claimed in either of claims 2 and 3, characterized in that the first capacitor

face (18) is arranged on the surface of the printed circuit board (5).

5. The interference suppression device as claimed in claim 4, characterized in that the printed circuit board (5) has two further capacitor faces (13, 21), which lie one above the other and which are electrically insulated from one another, for the purpose of forming a further capacitor (22) for the same plug element (8), the third capacitor face (13) being electrically connected to the plug element (8) and the fourth capacitor face (21) being electrically connected to the housing potential.

6. The interference suppression device as claimed in one of claims 2 to 5, characterized in that the fourth capacitor face (21) is arranged on the surface of the printed circuit board (5).

7. The interference suppression device as claimed in either of claims 5 and 6, characterized in that the first and the fourth capacitor faces (18, 21) are conductively connected to one another by means of plated-through holes which enclose between them the second and the third capacitor faces (12, 13) and preferably extend approximately on the plane of the housing wall.

8. The interference suppression device as claimed in one of claims 2 to 7, characterized in that one or more of the capacitor faces are capacitor coatings on the printed circuit board.

9. The interference suppression device as claimed in one of the preceding claims, characterized in that the plug element(s) or the capacitor faces (12) which are conductively connected to the plug elements are connected to the circuit via signal lines (15).

10. The interference suppression device as claimed in claim 9, characterized in that the signal lines are layer lines applied to the printed circuit board.

11. The interference suppression device as claimed in one of the preceding claims, characterized in that the opening (3) in the housing (1) tightly encloses the printed circuit board (5) passed through it.

12. The interference suppression device as claimed in claim 11, characterized in that the opening region of the housing (1) is in conductive contact with a first and/or fourth capacitor face (18, 21), which is/are arranged on the surface of the printed circuit board (5), of the capacitor (19, 22).

13. The interference suppression device as claimed in claim 11, characterized in that the opening region of the housing (1) bears in a resilient manner against the first and/or fourth capacitor face (18).

14. The interference suppression device as claimed in either of claims 11 and 12, characterized in that the opening region of the housing is connected to the first and/or fourth capacitor face by means of a connecting element, in particular by means of a rivet.

15. The interference suppression device as claimed in claim 11, characterized in that the opening region of the housing is connected in an interlocking manner to the first and/or fourth capacitor face.

16. The interference suppression device as claimed in claim 15, characterized in that part of the opening region of the housing is inserted in a corresponding cutout in the first and/or fourth capacitor face with a press fit.

17. The interference suppression device as claimed in one of claims 11 to 16, characterized in that the opening region of the housing (1) is conductively connected to the first and/or fourth capacitor face (18, 21) by adhesive bonding or soldering.

18. The interference suppression device as claimed in claim 11, characterized in that the housing is capacitively coupled to the first and/or fourth capacitor face.

19. The interference suppression device as claimed in one of the preceding claims, characterized in that the capacitor (19) and/or the further capacitor (22) is/are connected to the circuit via an interference suppression capacitor (16).

20. The interference suppression device as claimed in one of the preceding claims, characterized in that the housing wall (2) has shielding arms (27, 28) lying adjacent to one another in the region of the opening (3), said shielding arms (27, 28) being short in the regions of the capacitors (19, 22) extending from the housing exterior (10) to the housing interior (4) and resting with their free ends on the first capacitor face (18), and in that the shielding arms (28) are long in the regions free of capacitors (19, 22) extending from the housing exterior (10) to the housing interior (4) and extend through through-openings (30) in the printed circuit board (5) until they come to bear with their free ends against a wall part of the housing (1).

21. The interference suppression device as claimed in claim 20, characterized in that the shielding arms (27, 28) bear on the first capacitor face (18) and the wall of the housing (1) with resilient prestress.

22. The interference suppression device as claimed in either of claims 20 and 21, characterized in that the housing wall (2, 23'') is in the form of a stamped/bent part in the region of the opening (3).

23. The interference suppression device as claimed in one of the preceding claims, characterized in that that part (9) of the printed circuit board (5) which is located in the housing exterior (10) and capacitors (19, 22) as well as the plug elements (8) are arranged in an outer, electrically conductive housing chamber (24, 24', 24'').